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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,204	09/02/2003	Yo Yanagida	06753.0564	1712

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EXAMINER	
CAVALLARI, DANIEL J	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/652,204	YANAGIDA ET AL.	
	Examiner	Art Unit	
	Daniel J. Cavallari	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/2/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 9/2/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

The drawings are objected to for the following reasons:

Figure 1 has been disclosed in the specification as "a configuration of an ECU 100 which is now on file". This statement is taken as a disclosure of prior art and therefore should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Figures 6 & 7 do not correctly represent the circuit of Figure 5. Figure 6 is disclosed as "a graph showing an input signal waveform in an inverter circuit

constituting the waveform shaper" and Figure 7 is "a graph showing a signal waveform of incoming data after waveform shaping". This being the case, the inverter would invert component c to a low value and component d to a positive value. This, however, is the exact opposite of what is shown in figures 6 and 7. The drawings should be changed to correctly represent the circuit.

Specification

The specification is objected to because it fails to disclose the device of figure 5 in a way which matches its performance of figures 6 & 7. Figure 6 is disclosed as "a graph showing an input signal waveform in an inverter circuit constituting the waveform shaper" and Figure 7 is "a graph showing a signal waveform of incoming data after waveform shaping" (See Pages 7 & 8). This being the case, the inverter would invert component c to a low value and component d to a positive value. This, however, is the exact opposite of what is shown in figures 6 and 7. The drawings should be changed to correctly represent the circuit.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claim includes the limitation of a logic circuit comprising a comparator however the drawings (Figure 5) and specification only disclose an inverter (63). The specification fails to disclose the logic circuit in such a way as to enable one skilled in the art to make or use the invention using a comparator. Because of the 112 problems with this claim, no art can be applied.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 contains the limitation of "dulling a signal". It is unclear to the examiner what is meant by "dulling a signal". The word "dull" is not commonly used to refer to signals and is not given a clear definition in the specification (See Page 12). However, the examiner notes that "dulling" a signal is achieved by means of a low pass filter and will interpret the claim as best understood in which "dulling a signal" is meant as "attenuating".

Claim 1 further claims a detector configured to detect the communication signal and to extract incoming data including a digital signal. It is unclear to the examiner how the input signal is digital. The low pass filter of components 61 & 62 do not constitute a digital to analog converter and therefore the analog voltage output from the filter (shown in Figure 7) must have come from an analog input. Although the analog signal may represent a digital signal, it appears analog in form on the power line (102) hence the need for the analog to digital conversion that takes place by inverter (63). If the signal were already in true digital form at the detector (5), no further conversion would be required.

Claim 1 will be examined as best understood in which the incoming signal is analog.

Claim 6 recites the limitation of "the threshold value set to an intermediate value" is unclear as the "intermediate value" is a range rather than a single, specific voltage. The claim will be examined as best understood in which the threshold is a single value.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6, & 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nerone et al. (US 6,800,957) and Riley (US 5,870,401).

Nerone et al. (*hereinafter referred to as Nerone*) teaches:

- A detector configured to detect a communication signal superimposed on a direct-current power line (3) (See Figure 1 & Column 3, Lines 30-36) and extract the incoming data
- A waveform shaper read on by the data receiver (13) and data decoder (21) which receive the data from the detector (12) and produce an output to be used by the power converter (5) or load (25) (See Figure 1 & Column 3, Lines 30-51)
- Converting an analog signal into a digital signal (See Figure 3A & 3B)

Nerone fails to teach attenuating a waveform signal and converting the incoming analog signal into a digital signal based on a given threshold. Riley teaches a signal conditioning circuit used to produce a digital signal from an analog input (See Figure 3A). The conditioning circuit includes an anti-aliasing filter, read on by the low pass filter, capacitor (C) and resistor (R) of Figure 3A, a hysteresis circuit (126) for accepting different voltage level ranges at its input, and a digital output (152) from the logic circuit (126) in which the hysteresis circuit sets a minimum voltage level threshold representative of the input device being in one logic state and a maximum voltage threshold representative of the input device being in another logic state (See Abstract &

Column 7, Line 43 to Column 8, Line 42). The thresholds (VTL & VTH) being chosen for comparators (146 & 148) to produce a digital output (LOTRIP & HITRIP).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the signal conditioning circuit of Riley into the power line communication device taught by Nerone in place of the data receiver (13) and data decoder (21) in which the signal is extracted by the decoupler (12) (See Figure 1) and inputted into the signal conditioning circuit of Riley through input (130) (See Figure 3A). The motivation would have been to utilize the systems ability to select varies input voltage ranges as the input making it more versatile (See Column 7, Line 66 to Column 8, Line 10).

The preamble "for a vehicle" is merely a statement of intended use. The preamble is not part of the limitation when the claim is drawn to a structure and the portion of the claim following the preamble is merely a description of the structure not dependant for completeness upon the introductory clause. Catalina Mktg. Int 'l v. Coolsavings.com, Inc., 289 F.3d 801, 808, 62 USPQ2d 1781, 1785 (Fed. Cir. 2002).

Furthermore, Nerone et al. teaches a power line communication device for a vehicle (See Column 1, Lines 5-11).

In regard to Claims 6 & 7

The conditioning circuit taught by Riley further includes a threshold value (VTL) which is an intermediate value of an operating value (36-42V or 12V-14V) (See Nerone, Abstract). Riley fails to explicitly teach where the threshold is set to 2.5V.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to create a threshold of 2.5 volts since it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). The threshold is merely a variable which can be optimized by the parameters of either the voltage applied to the hysteresis circuit (126) or the resistor value used (See resistor V225) for threshold VTL in which values of 1.25, 2.25, 3.75, and 6.75 are used.

The motivation would have been to select a value which produced the optimal digital control signal from the comparators for the device being controlled.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Yanagida et al. (US 2004/0207626) teaches a power line communication device for a vehicle.

- Yanagida et al. (US 2004/0207263) teaches a power line communication device for a vehicle.
- Akiyaya et al. (US 2003/0076221 A1) teaches a data over power line vehicle communication system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Cavallari whose telephone number is (571)272-8541. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

December 9, 2005

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
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